In The Specification:

Please amend paragraph [0005] as follows:

[0005] Dynamic random access memory (DRAM) is a type of ~~non-volatile~~ nonvolatile and easy-to-access memory mostly for holding operating data in a computer. Typically, a DRAM consists of an array of cells each comprising a metal-oxide-semiconductor (MOS) transistor and a capacitor. The source/drain regions of the transistor are electrically connected to a capacitor and a bit line respectively. At present, DRAM capacitors are classified into stacked capacitor or trench capacitor. A stacked capacitor is formed over the transistor and a trench capacitor is formed below the transistor.

Please amend paragraph [0015] as follows:

[0015] Figs. 1 through 8 are diagrams showing the steps for producing a DRAM structure according to one preferred embodiment of this invention. In Figs. 1, 2 and 7, the sub-diagrams with a label (C) are top views and the sub-diagrams with a label (A)/(B) are cross-sectional views along line A-A'/B-B' of the one labeled (C). As shown in Fig. 1(A)/(B)/(C), a substrate 100 such as a P-type monocrystalline silicon substrate is provided. Thereafter, a pad oxide layer 102 and a hard mask layer 104 are formed over the substrate 100. The hard mask layer ~~106~~ 104 is a silicon nitride layer, for example. The hard mask layer 104, the pad oxide layer 102 and the substrate 100 are sequentially patterned to form a plurality of trenches 110 in the substrate 100. The trenches 110 are configured to form an eight F-square folded bit line DRAM layout detailed in U.S. Patent

No. 5,874,758. In the eight F-square folded bit line DRAM layout, each area for forming an active region 130 is enclosed by four pairs of trenches 110 and each pair of trenches 110 is also enclosed by four areas for forming active regions 130. In addition, each area for forming an active region 130 has a pair of trenches in the Y direction located underneath a subsequently formed word line 134.

Please amend paragraph [0018] as follows:

[0018] As shown in Fig. 3(A)/(B), the dielectric layer 118 above the conductive layer 116 and the hard mask layer 104 ~~are~~ is removed and then another conductive material is deposited into the trenches 110 to form conductive layers 124 that expose a portion of the dielectric layer 118. The conductive layer ~~116~~ 124 is an N-type polysilicon layer, for example. Thereafter, the dielectric layers 118 above ~~than~~ the conductive layers 124 are removed to form collar dielectric layers 118a.

Please amend paragraph [0019] as follows:

[0019] As shown in Fig. 4(A)/(B), another conductive material is deposited into the trenches 110 to form conductive layers 126 with a top surface below the top surface of the substrate 100. The conductive material is N-type polysilicon, for example. The conductive layers 126 ~~serves~~ serve as an electrical connection between the inner electrode 116 and the source/drain region of a subsequently formed access transistor.

Please amend paragraph [0024] as follows:

[0024] In addition, Figs. 7 and 8 are also sectional views of a DRAM structure according to one preferred embodiment of this invention. The DRAM has a conventional eight F-square folded bit line buried strap structure. However, doped regions 122 are also incorporated in the design in this invention. The doped region 122 has a conductive type identical to the substrate 100. The DRAM structure comprises a substrate 100, active regions 130 surrounded by an isolation region 128, trenches 110, word lines 134, (common) source/drain regions 142, contacts 146, bit lines 148 and doped regions 122. The substrate 100 has a plurality of trenches 110. Each trench 110 encloses a capacitor comprising an external electrode 112, a capacitor dielectric layer 114 and an inner electrode 116. A pair of trenches 110 is ~~position~~ positioned on all four sides of each active region 130. Among the pairs of trenches 110 on the left and right side of the active region 130, the capacitor inside one of the trenches 110 is electrically coupled to the active region 130. Furthermore, among the pairs of trenches 110 on the front and back sides of the active region 130, the capacitors inside the trenches 110 are electrically coupled to other active regions 130 (refer to Fig. 1). In addition, a pair of neighboring word lines 134 passes through the active region 130 as well as the pair of front and back trenches 110. The word lines 134 run in a first direction. The areas within the active region 130 covered by the pair of word lines 134 form two channel regions. The doped regions 122 are formed on the two sides of each channel region adjacent to the isolation region 128. The active region 130 between the two word lines 134 has a common source/drain region 142 electrically connected to the bit line 148 running in a second

direction. The active region 130 also has two source/drain regions 142 on the outer edge of the two word lines 134 with each source/drain region 142 electrically connected to a corresponding capacitor.